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U.S. UTILITY Patent Application

PATENT NUMBER and

6671112

6671112

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10023769	12/21/2001	713	39	2432	HOLDER

**APPLICANTS: Murakami Hiroko; Sawada Masaru; Nakano Manabu; Kikuta Kazuyoshi;
360 2651

**CONTINUING DATA VERIFIED:

THIS APPLICATION IS A DIV OF 09/192,497 11/17/1998 PAT 6,377,416 RH 8/6/03
WHICH IS A DIV OF 08/691,411 08/02/1999 PAT 5,870,591 RH 8/6/03

**FOREIGN APPLICATIONS VERIFIED:

JAPAN 7-206223 08/11/1995 RH

JAPAN 7-212206 08/21/1995 RH

JAPAN 7-254169 09/29/1995 RH

PG-PUB DO NOT PUBLISH ☐

RESCIND ☐

Foreign priority claimed

☒ yes ☐ no

35 USC 119 conditions met

☒ yes ☐ no

Verified and Acknowledged Examiners' initials

RH

ATTORNEY DOCKET NO.

1076.1023D2

TITLE: Semiconductor integrated circuit device

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

11-20-3 Formal Drawings (37 sheets) set 1 3-29-2

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
8.12.03		Total Claims 23	Print Claim for O.G. 1
ISSUE FEE		DRAWING	
Amount Due 1300	Date Paid 11-4-03	Sheets Drwg. 37	Figs. Drwg. 44
		Print Fig. 28	
<input type="checkbox"/> TERMINAL DISCLAIMER		Application Examiner	
		PREPARED FOR ISSUE	
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ISSUE FEE IN FILE

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